

1     CLAIMS:

2           1.     A method of forming an isolation trench in a semiconductor  
3     comprising:

4           forming a first isolation trench portion having a first depth and  
5     having a first sidewall intersecting a surface of the semiconductor at a  
6     first angle;

7           forming a second isolation trench portion within and extending  
8     below the first isolation trench portion, the second isolation trench  
9     portion having a second depth and including a second sidewall intersecting  
10    the first sidewall at an angle with respect to the surface that is greater  
11    than the first angle; and

12          filling the first and second isolation trench portions with dielectric  
13    material.

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15          2.     The method of claim 1, wherein forming a second isolation  
16    trench portion includes forming the second angle to be between eighty  
17    and ninety degrees.

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19          3.     The method of claim 1, wherein forming a first isolation  
20    trench portion includes forming the first angle to be in a range of from  
21    about thirty degrees to about seventy degrees and forming a second  
22    isolation trench portion includes forming the second angle to be more  
23    than eighty degrees.

1           4.     The method of claim 1, wherein forming an isolation trench  
2 in a semiconductor comprises forming an isolation trench in silicon.

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4           5.     The method of claim 1, wherein forming a first isolation  
5 trench portion comprises:

6                 forming a silicon nitride layer on the semiconductor surface;

7                 forming a masking layer having an opening disposed therein atop  
8 the silicon nitride layer, the opening including sidewalls;

9                 plasma etching through the silicon nitride layer using conditions that  
10 also deposit a polymer on the sidewalls;

11                continuing etching for a predetermined time interval after the  
12 silicon nitride layer has been broached and continuing to deposit polymer  
13 on the sidewalls; and

14                stopping the etching and depositing at the end of the  
15 predetermined time interval.

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17           6.     The method of claim 5, wherein etching and depositing  
18 comprises:

19                 providing a mixture of gasses chosen from a group consisting of  
20  $\text{CF}_4$ ,  $\text{CHF}_3$ ,  $\text{CH}_2\text{F}_2$  and  $\text{C}_2\text{F}_8$ ; and

21                 supplying radio frequency excitation to the mixture.  
22  
23

1           7.    The method of claim 5, wherein etching and depositing  
2 comprises:

3           providing fluorocarbon gases; and

4           supplying radio frequency excitation to the mixture.  
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6           8.    The method of claim 1, wherein forming the first isolation  
7 trench portion comprises plasma etching the first isolation trench portion  
8 using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$   
9 to 0.67.  
10

11           9.    The method of claim 1, wherein forming the first isolation  
12 trench portion comprises:

13           forming a silicon nitride layer on the semiconductor surface;

14           forming a masking layer having an opening disposed therein atop  
15 the silicon nitride layer, the opening including sidewalls;

16           plasma etching through the silicon nitride layer using gases including  
17  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to 0.67;

18           depositing a polymer on the sidewalls during plasma etching;

19           continuing etching for a predetermined time after the silicon nitride  
20 layer has been broached and continuing depositing polymer on the  
21 sidewalls; and

22           stopping etching and depositing when the predetermined interval  
23 ends.

10. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

11. The method of claim 1, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

12. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

13. A method of forming an isolation trench in a surface of a silicon wafer comprising:

forming a mask on the surface, the mask including an opening and sidewalls; and

etching the silicon surface using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$  to form a first isolation trench portion.

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1           14. The method of claim 13, wherein etching the silicon surface  
2 includes forming a first isolation trench portion having a first sidewall  
3 that intersects the silicon surface at an angle in a range of from about  
4 thirty degrees to about seventy degrees.

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6           15. The method of claim 14, wherein forming a first isolation  
7 trench portion comprises forming a first isolation trench portion including  
8 a sidewall at least some of which forms a substantially straight linear  
9 segment.

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11           16. The method of claim 13, further comprising forming a second  
12 isolation trench portion within and extending below the first isolation  
13 trench portion, the second isolation trench portion including a second  
14 sidewall intersecting the first sidewall at an angle with respect to the  
15 surface that is greater than the first angle.

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17           17. The method of claim 16, wherein forming a first isolation  
18 trench portion comprises forming a first isolation trench portion having  
19 a first depth of between five and fifty percent of a total trench depth.

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1 18. The method of claim 17, further comprising:  
2 filling the first and second isolation trench portions with dielectric  
3 material; and  
4 planarizing the dielectric material filling the first and second  
5 isolation trench portions.

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7 19. The method of claim 13, wherein forming a mask comprises:  
8 forming a silicon nitride layer on the semiconductor surface; and  
9 forming a masking layer having an opening disposed therein atop  
10 the silicon nitride layer, the opening including sidewalls.

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12 20. The method of claim 19, wherein etching the surface  
13 comprises:

14 plasma etching through the silicon nitride layer;  
15 continuing etching for a predetermined time interval after the  
16 silicon nitride layer has been broached and continuing to deposit polymer  
17 on the sidewalls; and

18 stopping the etching and depositing at the end of the  
19 predetermined time interval.  
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1           21.    The method of claim 19, further comprising forming a second  
2 isolation trench portion within and extending below the first isolation  
3 trench portion, the second isolation trench portion having a second depth  
4 and including a second sidewall intersecting the first sidewall at an angle  
5 with respect to the surface that is greater than the first angle.

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1           22. A method of forming an isolation trench-isolated transistor  
2 comprising:

3           forming first and second isolation trenches disposed to a respective  
4 side of a portion of silicon, forming the first and second isolation  
5 trenches comprising:

6                 forming a mask on the surface, the mask including first and  
7 second openings corresponding to the first and second isolation  
8 trenches;

9                 forming a first isolation trench portion in each of the first  
10 and second openings, each first isolation trench portion having a  
11 first depth and having a first sidewall intersecting a surface of the  
12 semiconductor at a first angle; and

13                 forming a second isolation trench portion within and  
14 extending below each of the first isolation trench portions, the  
15 second isolation trench portions having a second depth and  
16 including a second sidewall intersecting a respective one of the first  
17 sidewalls at an angle with respect to the surface that is greater  
18 than the first angle; the method further comprising:

19                 filling the first and second isolation trench portions with dielectric  
20 material;

21                 forming a gate extending across the silicon portion from the first  
22 isolation trench to the second isolation trench; and

23                 forming source and drain regions extending between the first and



1 second isolation trench portions, the source region being disposed adjacent  
2 one side of the gate and the drain region being disposed adjacent  
3 another side of the gate that is opposed to the one side.  
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5 23. The method of claim 22, wherein forming a first isolation  
6 trench portion comprises etching the silicon surface using gases including  
7  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ .  
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9 24. The method of claim 22, wherein forming a mask comprises:  
10 forming a silicon nitride layer on the semiconductor surface; and  
11 forming a masking layer having an opening disposed therein atop  
12 the silicon nitride layer, the opening including sidewalls.  
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14 25. The method of claim 22, wherein forming a first isolation  
15 trench portion comprises:  
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17 plasma etching through the silicon nitride layer using conditions that  
18 also deposit a polymer on the sidewalls;  
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20 continuing etching for a predetermined time after the silicon nitride  
21 layer has been broached and continuing to deposit polymer on the  
22 sidewalls; and  
23

24 stopping the etching and depositing at the end of the  
25 predetermined interval.

1           26. The method of claim 25, wherein plasma etching comprises  
2 etching using gases including  $\text{CF}_4$  and  $\text{CHF}_3$  in a ratio of  
3  $\text{CF}_4/\text{CHF}_3 = 0.11$  to  $0.67$ .  
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5           27. The method of claim 22, wherein forming a first isolation  
6 trench portion comprises forming a first isolation trench portion having  
7 a first sidewall intersecting a surface of the semiconductor at an angle  
8 in a range of from about thirty degrees to about seventy degrees.  
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10           28. The method of claim 22, wherein forming a first isolation  
11 trench portion comprises forming a first isolation trench portion including  
12 a sidewall at least some of which forms a substantially straight linear  
13 segment.  
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15           29. The method of claim 27, wherein forming a second isolation  
16 trench portion comprises forming a second isolation trench portion having  
17 a second sidewall forming an angle of more than eighty degrees with the  
18 surface.  
19

20           30. The method of claim 22, wherein forming a first isolation  
21 trench portion comprises forming a first isolation trench portion having  
22 a first depth of between five and fifty percent of a total trench depth.  
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1           31. The method of claim 30, further comprising planarizing the  
2 dielectric material filling the first and second isolation trench portions.

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4           32. The method of claim 22, wherein forming a gate comprises  
5 forming a gate comprising polysilicon.

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33. A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

1           34. The trench-isolated transistor of claim 33, wherein the first  
2 isolation trench portion comprises a sidewall at least some of which forms  
3 a substantially straight linear segment.  
4

5           35. The trench-isolated transistor of claim 33, wherein the second  
6 angle is between eighty and ninety degrees.  
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8           36. The trench-isolated transistor of claim 33, wherein the first  
9 angle is in a range of from about thirty degrees to about seventy degrees  
10 and the second angle is more than eighty degrees.  
11

12           37. The trench-isolated transistor of claim 33, wherein the first  
13 isolation trench portion has a first depth of between five and fifty  
14 percent of a total trench depth.  
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16           38. The trench-isolated transistor of claim 33, wherein the  
17 dielectric material filling the first and second isolation trench portions has  
18 a planar surface.  
19

20           39. The trench-isolated transistor of claim 33, wherein the first  
21 angle is in a range of from about thirty degrees to about seventy  
22 degrees.  
23

1           40. The trench-isolated transistor of claim 39, wherein the second  
2 angle is in a range of from eighty to ninety degrees.

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4           41. The trench-isolated transistor of claim 33, wherein the  
5 transistor is formed as a part of a memory integrated circuit.

6  
7           42. A trench isolation structure formed in a semiconductor  
8 comprising:

9           a first isolation trench portion having a first depth and having a  
10 first sidewall intersecting a surface of the semiconductor at a first angle;

11           a second isolation trench portion within and extending below the  
12 first isolation trench portion, the second isolation trench portion having  
13 a second depth and including a second sidewall intersecting the first  
14 sidewall at an angle with respect to the surface that is greater than the  
15 first angle; and

16           a dielectric material filling the first and second isolation trench  
17 portions.

18  
19           43. The trench isolation structure of claim 42, wherein the first  
20 isolation trench portion comprises a sidewall at least some of which forms  
21 a substantially straight linear segment.

1           44. The trench isolation structure of claim 42, wherein the first  
2 angle is in a range of from about thirty degrees to about seventy degrees  
3 and the second angle is more than eighty degrees.  
4

5           45. The trench isolation structure of claim 42, wherein the first  
6 angle is in a range of from about thirty degrees to about seventy  
7 degrees.  
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9           46. The trench isolation structure of claim 42, wherein the first  
10 isolation trench portion has a first depth of between five and fifty  
11 percent of a total trench depth.  
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13           47. The trench isolation structure of claim 42, wherein the trench  
14 isolation structure is formed in a memory integrated circuit.  
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1           48. A memory cell including:  
2           a capacitor;  
3           a trench-isolated transistor having a gate, a drain and a source, the  
4 source being coupled to one terminal of the capacitor, the trench-isolated  
5 transistor including:  
6           first and second isolation trenches each disposed on a respective  
7 side of a portion of silicon, the first and second isolation trenches each  
8 comprising:  
9           a first isolation trench portion having a first depth and  
10 having a first sidewall intersecting a surface of the silicon at a first  
11 angle;  
12           a second isolation trench portion within and extending below  
13 the first isolation trench portion, the second isolation trench portion  
14 having a second depth and including a second sidewall intersecting  
15 the first sidewall at an angle with respect to the surface that is  
16 greater than the first angle; and  
17           a dielectric material filling the first and second isolation  
18 trench portions;  
19 the transistor further comprising:  
20           a gate extending across the silicon portion from the first  
21 isolation trench to the second isolation trench; and  
22           source and drain regions extending between the first and  
23 second isolation trench portions and across the silicon portion, the



source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

49. The memory cell of claim 48, wherein the gate comprises polysilicon.

50. The memory cell of claim 48, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

51. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

52. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.



1 55. A DRAM comprising:  
2 address decoding circuitry;  
3 a group of bitlines coupled to the address decoding circuitry and  
4 extending in a first direction;  
5 a group of wordlines coupled to the address decoding circuitry and  
6 extending in a second direction, each wordline in the group of wordlines  
7 intersecting each of the bitlines in the group of bitlines once at an  
8 intersection;  
9 a plurality of memory cells each disposed at one of the  
10 intersections, each memory cell comprising:  
11 a capacitor;  
12 a trench-isolated transistor having a gate, a drain and a  
13 source, the source being coupled to one terminal of the capacitor,  
14 the trench-isolated transistor including:  
15 first and second isolation trenches each disposed on a  
16 respective side of a portion of silicon, the first and second isolation  
17 trenches each comprising:  
18 a first isolation trench portion having a first depth and  
19 having a first sidewall intersecting a surface of the silicon at  
20 a first angle;  
21 a second isolation trench portion within and extending  
22 below the first isolation trench portion, the second isolation  
23 trench portion having a second depth and including a second

1 sidewall intersecting the first sidewall at an angle with respect  
2 to the surface that is greater than the first angle; and  
3 a dielectric material filling the first and second isolation  
4 trench portions;

5 the transistor further comprising:

6 a gate extending across the silicon portion from the  
7 first isolation trench to the second isolation trench; and

8 source and drain regions extending between the first  
9 and second isolation trench portions and across the silicon  
10 portion, the source region being disposed adjacent one side  
11 of the gate and the drain region being disposed adjacent  
12 another side of the gate that is opposed to the one side;

13 each memory cell further including:

14 one bitline of the group of bitlines coupled to the drain; and  
15 one wordline of the group of wordlines coupled to the gate.

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17 56. The DRAM of claim 55, wherein the first isolation trench  
18 portion comprises a sidewall at least some of which forms a substantially  
19 straight linear segment.

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21 57. The DRAM of claim 55, wherein the gate comprises  
22 polysilicon.  
23

1           58. The DRAM of claim 55, wherein the first angle is in a range  
2 of from about thirty degrees to about seventy degrees and the second  
3 angle is more than eighty degrees.  
4

5           59. The DRAM of claim 55, wherein the first angle is in a range  
6 of from about thirty degrees to about seventy degrees.  
7

8           60. The DRAM of claim 55, wherein the first isolation trench  
9 portion has a first depth of between five and fifty percent of a total  
10 trench depth.  
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12           61. The DRAM of claim 55, wherein the dielectric material filling  
13 the first and second isolation trench portions includes a planar outer  
14 surface.  
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